

## WIRE BOND PADS

### DESCRIPTION

#### [Para 1] FIELD OF THE INVENTION

[Para 2] The present invention relates to the field of integrated circuit chips; more specifically, it relates to input/output (I/O) and power bonding pads for integrated circuit chips and method of fabricating the bonding pads.

#### [Para 3] BACKGROUND OF THE INVENTION

[Para 4] Many types of integrated circuit chips utilize wire bonding as a means connecting the integrated circuit chip to the next higher level of packaging, for example, for the chip connecting to a module. Wire bonding requires wire bond pads be placed on the periphery of the integrated circuit chip. Since wire bond pads are exposed to the ambient environment, sealing the edges of the wire bond pads is a requirement. Otherwise early failures and reliability problems can occur.

[Para 5] As integrated circuit chips have become smaller, feature (such as interconnect wire widths and spacing) sizes have been reduced and input/output (I/O) pin density has increased to increase productivity, but wire bond pads have not decreased in size or pitch (the center to center spacing of adjacent wire bond pads) proportionally to the decrease in chip and feature sizes. The industry has turned to other I/O pad types such as solder bump, that offer greater I/O density, though at a greater cost which reduces productivity.

[Para 6] Therefore, there is a need for a high density wire bond pad structure that offers increased I/O count without sacrificing reliability or impacting productivity.

#### [Para 7] SUMMARY OF THE INVENTION

**[Para 8]** A first aspect of the present invention is a method, comprising: providing a substrate; forming an electrically conductive layer on a top surface of the substrate; patterning the conductive layer into a plurality of wire bond pads spaced apart; and forming a dielectric layer on the top surface of the substrate in spaces between adjacent wire bond pads, top surfaces of the dielectric layer in the spaces coplanar with coplanar top surfaces of the wire bond pads.

**[Para 9]** A second aspect of the present invention is a method, comprising: (a) providing a substrate; (b) forming a passivation layer on a top surface of the substrate; (c) forming an electrically conductive layer on a top surface of the passivation layer; (d) patterning the conductive layer into a plurality of wire bond pads spaced apart, top surfaces of the wire bond pads coplanar; and (e) forming a dielectric layer on the top surface of the passivation layer in spaces between adjacent wire bond pads and on the top surfaces of the wire bond pads, the dielectric layer filling the spaces; and (f) removing the dielectric layer from the top surface of the wire bond pads, the top surface of the dielectric layer in the spaces coplanar with the top surfaces of the wire bond pads.

**[Para 10]** A third aspect of the present invention is a structure, comprising: a substrate; a plurality of wire bond pads on a top surface of the substrate, the wire bond pads spaced apart; and a dielectric layer on the top surface of the substrate in spaces between adjacent wire bond pads, top surfaces of the wire bond pads recessed below top surfaces of the dielectric layer in the spaces.

**[Para 11]** A fourth aspect of the present invention is a structure, comprising: a substrate; a plurality of wire bond pads on a top surface of the substrate, the wire bond pads spaced apart; and a dielectric layer on the top surface of the substrate in spaces between adjacent wire bond pads, top surfaces of the wire bond pads recessed below top surfaces of the dielectric layer in the spaces.

**[Para 12] BRIEF DESCRIPTION OF DRAWINGS**

**[Para 13]** The features of the invention are set forth in the appended claims. The invention itself, however, will be best understood by reference to the following detailed description of an illustrative embodiment when read in conjunction with the accompanying drawings, wherein:

**[Para 14]** FIG. 1 a plan view of a corner portion of an exemplary integrated circuit chip utilizing related art wire bond pads;

**[Para 15]** FIG. 2 is a partial cross-sectional view through line 2-2 of FIG. 1;

**[Para 16]** FIG. 3 a plan view of an integrated circuit chip utilizing wire bond pads according to a first embodiment of the present invention;

**[Para 17]** FIG. 4 is a partial cross-sectional view through line 4-4 of FIG. 3;

**[Para 18]** FIG. 5 is a partial cross-sectional view through line 5-5 of FIG. 3;

**[Para 19]** FIGs. 6A through 6J are partial cross-section views through line 4-4 of FIG. 3, illustrating fabrication of wire bond pads according to first, second and third embodiments of the present invention; and

**[Para 20]** FIGs. 7A through 7E are partial cross-section views through line 4-4 of FIG. 3, illustrating fabrication of wire bond pads according to fourth, fifth and sixth embodiments of the present invention.

## **[Para 21] DETAILED DESCRIPTION OF THE INVENTION**

**[Para 22]** FIG. 1 a plan view of a corner portion of an exemplary integrated circuit chip utilizing related art wire bond pads. In FIG. 1, an integrated circuit chip 100 has a terminal passivation layer 105 over a top surface of the integrated circuit chip. Openings 110 in terminal passivation layer 105 expose the top surface of wire bond pads 115. A periphery 116 of each opening 110 is contained within a periphery 117 of a corresponding wire bond pad 115. There is a web 118 of terminal passivation layer 105 between

adjacent wire bond pads 115. Wire bond pads 115 are arranged along a periphery 120 of integrated circuit chip 100 and separated by spaces 122. Wire bond pads 115 are electrically connected to electrically conductive wires 125 within integrated circuit chip 100 through vias 130.

[Para 23] FIG. 2 is a partial cross-sectional view through line 2-2 of FIG. 1. In FIG. 2, wire bond pads 115 are formed on a final passivation layer 135 on a substrate 140 (which includes wires 125 (see FIG. 1), additional wires and devices such as transistors and capacitors that form the circuit of integrated circuit chip 100. Terminal passivation layer 105 overlaps edge regions 142 of wire bond pads 115. Final passivation layer 135 includes, in the present example, a first dielectric layer 145 on top of substrate 140, a second dielectric layer 150 on top of first dielectric layer 145 and a third dielectric layer 155 on top of second dielectric layer 155. Terminal passivation layer 105 includes, in the present example, a first dielectric layer 160 on top of edges 142 of wire bond pads 115 and final passivation layer 135, a second dielectric layer 165 on top of first dielectric layer 160 and a third dielectric layer 170 on top of second dielectric layer 165.

[Para 24] Adjacent wire bond pads 115 are separated by space 122 having a width S1. Terminal passivation layer 105, between adjacent wire bond pads 115 has a width W1 and a thickness T. Dielectric layer 165 comprises a photo-sensitive polyimide and dielectric layer 165 is about 12 microns thick. Thick polyimide is required to ensure good sealing of the integrated chip from ambient environment, but also limits the minimum printable image size. For example, with about a 12 micron thick polyimide, the minimum value for W1 is about 8 microns. There is a further minimum overlap distance of terminal passivation layer 105 and wire bond pads 115 of L1 = about 3 microns. Together the W1 and L1 requirements result in a minimum value for S1 of about 2 microns.

[Para 25] The present invention results in wire bond pads that may be spaced closer together than heretofore possible.

[Para 26] FIG. 3 a plan view of an integrated circuit chip utilizing wire bond pads according to a first embodiment of the present invention. In FIG. 3, an integrated circuit chip 200 has a terminal passivation layer 205 over a top surface of the integrated circuit chip. Openings 210 in terminal passivation layer 205 expose the top surface of wire bond pads 215. Openings 210 extend across adjacent wire bond pads 210 and there is no “web” as illustrated in FIG. 1 and described *supra*. Sets of wire bond pads, each set including outer wire bond pads 215A and inner wire bond pads 215B are arranged in rows along the periphery 220 of integrated circuit chip 200 and separated by spaces 222. Outer wire bond pads are defined as wire bond pads having an adjacent inner wire bond pad of the same row on only one side of the outer wire bond pad. Inner wire bond pads are defined as wire bond pads having adjacent inner or outer wire bond pads of the same row on both of opposing sides of the inner wire bond pad. Each outer and inner wire bond pads 215A and 215B are electrically connected to corresponding electrically conductive wires 225 within integrated circuit chip 200 through a corresponding via 230. While single rows of wire bond pads are illustrated in FIG. 3, there may be two or more rows of wire bond pads per side of integrated circuit chip 200.

[Para 27] FIG. 4 is a partial cross-sectional view through line 4-4 of FIG. 3. In FIG. 4, outer wire bond pads 215A and inner wire bond pads 215B are formed on a final passivation layer 235 on substrate 240 (which includes wires 225 (see FIGs. 3 and 5), additional wires and devices such as transistors and capacitors that form the circuit of integrated circuit chip 200. Final passivation layer 205 includes, in the present example, a first dielectric layer 245 on top of substrate 240, a second dielectric layer 250 on top of first dielectric layer 245 and a third dielectric layer 255 on top of second dielectric layer 255. Final passivation layer 235 may include one layer, two layers, three layers as shown, or more layers. Materials and thicknesses for first dielectric layer 245, second dielectric layer 250 and third dielectric layer 255 are discussed *infra*.

[Para 28] In FIG. 4, terminal passivation layer 205 overlaps an edge region 242 of only outer wire bond pad 215A. Inner wire pads 215B are not overlapped by terminal passivation layer 205 in the section illustrated in FIG.

4. Outer wire bond pad 215A is separated from an adjacent inner wire bond pad 215B and adjacent inner wire bond pads 215B are separated from each other by spaces 222 having widths S2. However, between outer wire bond pad 215A and an adjacent inner wire bond pad 215B and between inner wire bond pads 215B, portions of first and second dielectric hard dielectric layers 260 and 265 fill up spaces 222. It should be understood, that wherever first and second dielectric hard dielectric layers 260 and 265 are indicated, they may be replaced with a single hard dielectric layer. Top surfaces 266 of first dielectric layer 260 and top surfaces 267 of second dielectric layer 265 are about coplanar with coplanar top surfaces 268 of outer and inner wire bond pads 215A and 215B.

[Para 29] The minimum value of space S2 is determined by the photolithography process used to pattern outer and inner wire bond pads 215A and 215B not by the photolithography process used to pattern the terminal passivation layer as is the case in FIG. 1. The wire bond pad photolithography process can print smaller images than the terminal passivation photolithography process because of the materials involved in the two processes and the minimum value of S2 thus may be significantly than that of S1. In one, example the minimum value of S2 is about 1 micron or less.

[Para 30] Given an example of a requirement to have a width of 40 microns of exposed wire bond pad, the wire bond array of FIG. 1 requires a 48 micron wire bond pitch (center to center spacing) when S1 = 2 microns and L1 = 3 microns, while the wire bond array of FIG. 3 requires a 41 micron wire bond pitch when S2 = 1 micron. This is a savings of about 15% in wire bond pitch.

[Para 31] Materials and thicknesses for first dielectric layer 260, second dielectric layer 265 and final dielectric layer 270 are discussed *infra*.

[Para 32] FIG. 5 is a partial cross-sectional view through line 5-5 of FIG. 3. In FIG. 5, via 230 is formed through passivation layer 235 and makes physical and electrical contact to wire 225. Wire 225 is illustrated as having a

core conductor 280 and a conductive liner 280. In one example, core conductor comprises copper and conductive liner 275 comprises layers of tantalum and tantalum nitride, the tantalum layer between the copper core and the tantalum nitride layer.

**[Para 33]** FIGs. 6A through 6J are partial cross-section views through line 4-4 of FIG. 3, illustrating fabrication of wire bond pads according to first, second and third embodiments of the present invention. In FIG. 6A, passivation layer 235 is formed on substrate 240 . Passivation layer 235 comprises first dielectric layer 255, second dielectric layer 245 and third dielectric layer 255 as described *supra*. In one example, first dielectric layer 245 comprises silicon nitride, second dielectric layer 250 comprises silicon oxide and third dielectric layer 255 comprises silicon nitride.

**[Para 34]** Between FIGs. 6A and 6B, vias 230 (see FIG. 5) not visible in section 4-4 are formed in passivation layer 235 by photolithographic and etch processes, including reactive ion etch (RIE), well known in the art.

**[Para 35]** In FIG. 6B an electrically conductive layer 285 is formed on a top surface of 290 of passivation layer 235. In one example, conductive layer 285 comprises, aluminum, aluminum copper alloy, a layer of aluminum covered by a layer of gold, copper, a layer of copper over a layer of tantalum, a layer of copper over layers of tantalum and tantalum nitride or combinations thereof. In one example, conductive layer 285 is about 0.5 microns to about 5 microns thick.

**[Para 36]** In FIG. 6C, a photolithographic process (depositing a photoresist layer, patterning the photoresist layer to expose portions of the underlying material, etching the underlying material, and removing the photoresist layer) is performed to form outer wire bond pad 215A and inner wire bond pads 215B separated by spaces 222. Because outer wire bond pad 215A and inner wire bond pads 215B are formed from the same conductive layer 285 (see FIG. 6B), top surfaces 295 of outer wire bond pad 215A and inner wire bond pads 215B are coplanar.

**[Para 37]** In FIG. 6D, first dielectric layer 260 is conformally deposited over top surfaces 295 of outer wire bond pad 215A and inner wire bond pads 215B and top surface 290 of passivation layer 235 as well as sidewalls 300 of outer wire bond pad 215A and inner wire bond pads 215B. Since a second dielectric layer 265 (see FIG. 6E) will be deposited in the next step, illustrated in FIG. 6E and described *infra*, first dielectric layer does not fill spaces 222 completely. However, if only one hard dielectric layer is used, then it is deposited with a sufficient thickness to fill spaces 222 to or above top surfaces 295 of outer wire bond pad 215A and inner wire bond pads 215B.

**[Para 38]** In FIG. 6E, second dielectric layer 265 is conformally deposited on a top surface 305 of first dielectric hard layer 260. In one example, first dielectric layer 260 comprises silicon oxide and second dielectric layer 265 comprises silicon nitride. The combined thicknesses of first and second dielectric layers 260 and 265 are chosen to fill spaces 222 to or above top surfaces 295 of outer wire bond pad 215A and inner wire bond pads 215B. The thickness of first dielectric layer 260 is chosen to be less than about half the width of spaces 222 (see FIG. 6B). The thickness of second dielectric layer 265 is chosen to be sufficient to fill any remaining region of spaces 222 to or above top surfaces 295 of outer wire bond pad 215A and inner wire bond pads 215B. For example, if the width of spaces 222 are about 1 micron sand the thickness of outer wire bond pad 215A and inner wire bond pads 215B is about 1.2 microns, then the total thickness of first and second dielectric layers 260 and 265 may be about 0.85 microns with one possible combination of thicknesses being about 0.45 microns of first dielectric layer 260 and about 0.4 microns of second dielectric layer 265.

**[Para 39]** Processing may continue to the processes and structures described in relation to FIG. 6F through 6J for the first, second and third embodiments of the present invention, or continue to the processes and structures described in relationship to FIG. 7A through 7D for the fourth, fifth and sixth embodiments of the present invention.

**[Para 40]** Continuing from FIG. 6E, in FIG. 6F, final dielectric layer 270 is applied to a top surface 310 of second dielectric layer 265. In one example, final dielectric layer 270 comprises photo-sensitive polyimide and is about 4 microns to about 20 microns thick. Photo-sensitive polyimide may be patterned directly, without the need to pattern a photo-resist layer first. In a second example, final dielectric layer 270 comprises polyimide and is about 4 microns to about 20 microns thick.

**[Para 41]** In FIG. 6G, third dielectric layer is patterned and opening 210 formed over outer wire bond pad 215A and inner wire bond pads 215B and now filled spaces 222. In the example of final dielectric layer 270 being photo-sensitive polyimide, the third dielectric layer is exposed to light through a mask and the third dielectric layer developed to form openings 210. In the example of final dielectric layer 270 being polyimide, a resist layer is applied over the third dielectric layer, the resist layer exposed to light through a mask, the resist layer developed, the third dielectric layer etched where not protected by the resist layer, and the resist layer removed.

**[Para 42]** In FIG. 6H, an RIE process (for example using a fluorine containing gas) is performed to remove first and second dielectric layers 260 and 265 from top surfaces 295 of outer wire bond pad 215A and inner wire bond pads 215B that are not protected by final dielectric layer 270. However, between outer wire bond pad 215A and an adjacent inner wire bond pad 215B and between inner wire bond pads 215B, portions of first and second dielectric layers 260 and 265 remain, filling up spaces 222 so that top surfaces 266 of first dielectric layer 260 and top surfaces 267 of second dielectric layer 265 are about coplanar with coplanar top surfaces 295 of outer and inner wire bond pads 215A and 215B. The structure illustrated in FIG. 6H constitutes the first embodiment of the present invention. Processing may now terminate or processing may continue to the processes described in reference to either of FIG. 6I or FIG. 6J.

**[Para 43]** Continuing from FIG. 6H, in FIG. 6I, first and second dielectric layers 260 and 265 in spaces 222 are recessed below top surfaces 295 of

outer and inner wire bond pads 215A and 215B. This may be accomplished by increasing the etch time of the etch described *supra* in reference to FIG. 6H, or by performing a second RIE process (for example using a fluorine containing gas). The structure illustrated in FIG. 6I constitutes the second embodiment of the present invention. Processing now terminates.

**[Para 44]** Continuing from FIG. 6H, in FIG. 6J, outer and inner wire bond pads 215A and 215B are recessed below top surfaces 266 of first dielectric layer 260 and top surfaces 267 of second dielectric layer 265 filling spaces 222. In the example that the wire bond pads comprise aluminum or aluminum alloy a RIE using a chlorine containing gas may be used. In the example that the wire bond pads comprise copper, an aqueous ammonium fluoride/hydrogen peroxide mixture may be used. The structure illustrated in FIG. 6J constitutes the third embodiment of the present invention. Processing now terminates.

**[Para 45]** Continuing from FIG. 6E, FIGs. 7A and 7E are partial cross-section views through line 4-4 of FIG. 3, illustrating fabrication of wire bond pads according to fourth, fifth and sixth embodiments of the present invention. In FIG. 7A a chemical-mechanical polish (CMP) process is performed to remove first and second dielectric layers 260 and 265 from over outer wire bond pad 215A and inner wire bond pads 215B, but leave spaces 222 filled with first and second dielectric layers 260 and 265 so top surfaces 266 of first dielectric layer 260 and top surfaces 267 of second dielectric layer 265 are about coplanar with coplanar top surfaces 295 of outer and inner wire bond pads 215A and 215B. Unlike the first three embodiments of the present invention there are no edges of outer wire bond pad 215A and inner wire bond pads 215B that are overlapped or covered by first and second dielectric layers 260 and 265 anywhere on the chip.

**[Para 46]** Processing may continue to the processes and structures described in relation to FIG. 7B for the fourth embodiment of the present invention or continue to the processes and structures described in relationship to FIG. 7D for the fifth and sixth embodiments of the present invention.

**[Para 47]** Continuing from FIG. 7A, in FIG. 7B, final dielectric layer 270 is applied to top surfaces 266 of first dielectric layer 260, top surface 267 of second dielectric layer 265 and to top surfaces 295 of outer and inner wire bond pads 215A and 215B and patterned as described *supra* in relation to FIGs. 6F and 6G. Final dielectric layer 270 is in direct contact with outer wire bond pad 215A over an edge region 315 of the outer wire bond pad. The structure illustrated in FIG. 7B constitutes the fourth embodiment of the present invention. Processing may now terminate or processing may continue to the processes described in reference to either of FIG. 7C or FIG. 7D.

**[Para 48]** Continuing from FIG. 7B, in FIG. 7C, outer and inner wire bond pads 215A and 215B are recessed so that top surfaces 320 of outer and inner wire bond pads 215A and 215B are below top surfaces 266 of first dielectric layer 260 and top surfaces 267 of second dielectric layer 265 filling spaces 222. The structure illustrated in FIG. 7B constitutes the fifth embodiment of the present invention. Processing now terminates.

**[Para 49]** Continuing from FIG. 7A, in FIG. 7D, outer and inner wire bond pads 215A and 215B are recessed so that top surfaces 320 of outer and inner wire bond pads 215A and 215B are below top surfaces 266 of first dielectric layer 260 and top surfaces 267 of second dielectric layer 265 filling spaces 222.

**[Para 50]** In FIG. 7E, final dielectric layer 270 is applied to top surfaces 266 of first dielectric layer 260, top surface 267 of second dielectric layer 265 and to top surfaces 320 of outer and inner wire bond pads 215A and 215B and patterned as described *supra* in relation to FIGs. 6F and 6G. Dielectric layer 270 is in direct contact with outer wire bond pad 215A over an edge region 315 of the outer wire bond pad. The structure illustrated in FIG. 7E constitutes the sixth embodiment of the present invention. Processing now terminates.

**[Para 51]** Thus, the present invention provides a high density wire bond pad structure that offers increased I/O count without sacrificing reliability or impacting productivity.

**[Para 52]** The description of the embodiments of the present invention is given above for the understanding of the present invention. It will be understood that the invention is not limited to the particular embodiments described herein, but is capable of various modifications, rearrangements and substitutions as will now become apparent to those skilled in the art without departing from the scope of the invention. Therefore, it is intended that the following claims cover all such modifications and changes as fall within the true spirit and scope of the invention.